[INTEGRATED CAPACITOR AND METHOD OF MAKING SAME]

Abstract of Disclosure

An integrated capacitor including a semiconductor substrate is disclosed. An outer vertical plate is laid over the semiconductor substrate. The outer vertical plate of a plurality of first conductive slabs connected vertically using multiple first via plugs. The outer vertical plate defines a grid area. An inner vertical plate is laid over the semiconductor substrate in parallel with the outer vertical plate and is encompassed by the grid area defined by the outer vertical plate. The inner vertical plate consists of a plurality of second conductive slabs connected vertically using multiple second via plugs. A horizontal conductive plate is laid under the outer vertical plate and inner vertical plate over the semiconductor substrate for shielding the outer vertical plate from producing a plate-to-substrate parasitic capacitance thereof. The inner vertical plate is electrically connected with the horizontal conductive plate using at least one third via plug.